PATENT
Attorney Docket No. 295.div

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Daniel E. Klausmeier, et al.	)	
	)	
Serial No.: Unassigned - Divisional Of Application Serial No. 09/427,299	)	Group Art Unit: Unassigned
	)	
Filed: December 17, 2001	)	Examiner: Unassigned
	)	
For: REARRANGEABLE SWITCH HAVING A NON-POWER OF TWO NUMBER OF PHYSICAL CENTER STAGES	)	

Assistant Commissioner for Patents
Washington, DC 20231

Sir/Madam:

PRELIMINARY AMENDMENT

The following preliminary amendment relates to the filing of a divisional application pursuant to 37 CFR 1.53(b) of the corresponding parent application, U.S. patent application number 09/427,299, filed 10/26/99. This preliminary amendment and remarks are respectfully submitted in connection with the above-identified application.

AMENDMENTS

IN THE WRITTEN DESCRIPTION

Please amend the title as follows:

-- REARRANGEABLE SWITCH HAVING A NON-POWER OF TWO NUMBER OF PHYSICAL CENTER STAGES --

Please replace the abstract with the following:

-- A switch is provided that includes three stages. The first stages has a plurality of switch circuits. The second stage has a plurality of switch circuits equal to N, where N is any integer other than a power of 2 and where the switch circuits can be logically configured into a logical configuration of a power of 2. The third stages includes a plurality of switch circuits. --

On page 4, replace the first and second full paragraphs with the following paragraphs:

--Fig. 1 illustrates a switch 100 consistent with an embodiment of the present invention. Switch 100 includes a plurality of inputs 110-1 to 110-256, which receive signals conforming to a given protocol from an external network; group the signals in frames suitable for processing in switch 100; and forward the signals to a first stage of switch circuits 112-1 to 112-32. The data signals are routed through these switch circuits and passed to a second stage of switch circuits 114-1 to 114-22, which further route the data signals. A third stage of switch circuits 116-1 to 116-32 direct the data to desired outputs 118-1 to 118-256, which supply the data signals to an external network, but typically in the protocol in which the signals were input to switch 100.

Fig. 2 illustrates input 110-1 in greater detail. Remaining inputs 110-2 to 110-256 typically have a similar construction as input 110-1. Data is generally supplied to input 110-1 as optical signals conforming to a Synchronous Optical Network (SONET) protocol at a rate of approximately 2.5 Gbit/sec. A receiver circuit, including for

example, photodetector 210 converts the received optical signals into corresponding electrical signals. A conventional clock and data recovery circuit 212 appropriately shapes the electrical signals and extracts a clock signal for timing purposes. A framer circuit is coupled to the output of the clock and data recovery circuit, for grouping the received data into frames suitable for processing within switch 100. --

On page 5, replace the second and third full paragraphs with the following paragraphs:

--By way of introduction, switches can be classified into one of two categories, space division and time division. Space division switches can be implemented as crossbar switches having m input and n outputs and mn crosspoints (m and n are integers). By making an electrical contact via a crosspoint between a horizontal input bus and a vertical output bus, a connection can be made between the associated input and output, respectively.

Instead of using a space division switch, however, time division switching techniques can also be applied for interconnecting inputs and outputs. A so-called time slot interchanger (TSI) can be used for such purposes. A TSI includes a buffer which reads from a single input and writes to a single output. The input is framed into m fixed-length time slots. The information in each input time slot is read sequentially into consecutive time slots (cyclically) of a buffer of m slots. The output is framed into n time slots, and information from the appropriate slot in the buffer is transmitted onto a corresponding output slot. Thus, over the duration of an output frame, the content of the buffer is read in predetermined manner according to a read-out sequence so that the information in each slot of the input frame is rearranged into the appropriate slot in the

output frame. As a result, each time slot is interchanged. ---

On page 6 and 7, please replace the full paragraph beginning at the bottom of page 6 and ending at the top of page 7 with the following paragraph:

-- An example of the steps carried out by the Looping Algorithm will next be described with reference to Fig. 4(c). In a first step, an unconnected input of 2 x 2 switch 420 in stage 406 is coupled, via upper switch 402, to desired output of 2 x 2 switch 423 in stage 408. The adjacent output of switch 422 423 is then coupled to a desired input, e.g., an input of switch 421, through lower switch 404. The 2 x 2 switch 421 in stage 406 then is coupled to the adjacent input of switch 421 through the upper switch 402 (loop forward) to an output of switch 422 in stage 408. An adjacent output of switch 422 is coupled to an input of stage 406 switch 420 through lower switch 404 (loop back). This process is repeated until both inputs of switch 420 are connected to corresponding outputs. This completes the loop of the Looping Algorithm. Next, another unconnected input of a 2 x 2 switch in stage 406 is chosen and the above referenced steps are repeted to complete the loop. When no more unconnected inputs are free, the Algorithm terminates.--

On page 8, please replace the first full paragraph with the following paragraph:

--Fig. 6 illustrates one of the switch banks shown in Fig. 5. Each bank includes two sub-stages 610 and 620 that have P 2 x 2 switches, where P is the width of the bus coupled to the inputs of each bank, e.g. P = 384 for the bank of stage 510, 192 for the banks of stage 512, 96 for the banks of stage 514, 48 for the banks of stage 516, 24 for

the banks of stage 518, and 12 for the banks of stage 520. Connections between each of the 2 x 2 switches are further illustrated in Fig. 6. These connections are consistent with the requisite hardware connections within each of switch circuits 112-1 to 112-32.--

IN THE CLAIMS:

Please cancel claims 1-15 without prejudice or disclaimer to the subject matter contained therein.

Please add the following new claims:

16. A rearrangeable, non-blocking switch, comprising:

a first stage including a plurality of first switch circuits, each of said plurality of first switch circuits including a plurality of inputs and a plurality of outputs;

a second stage including a plurality of second switch circuits, each of said plurality of second switch circuits including a plurality of inputs, each of which being respectively coupled to one of said plurality of outputs of each of said plurality of first switch circuits, and a plurality of outputs, a number of said plurality of second switch circuits equaling N, where N is an integer other than a power of 2; and

a third stage including a plurality of third switch circuits, each of said plurality of third switch circuits including a plurality of inputs and a plurality of outputs, each of said plurality of inputs of each of said plurality of third switch circuits being coupled to a respective one of said plurality of outputs of each of said plurality of second switch circuits,

wherein at least some of said plurality of second switch circuits are each configured as a plurality of logical switch circuits.

17. A switch in accordance with claim 16, wherein at least one of the plurality of logical switch circuits does not carry data in order to configure the at least some of said plurality of second switch circuits as n logical switch circuits, where n is a power of 2.

18. A switch in accordance with claim 16, wherein a Looping Algorithm is used as a control algorithm for the switch.

19. A switch in accordance with claim 16, wherein each of said plurality of first and third switch circuits are configured to be logically represented as respective groupings of 2 x 2 switches.

20. A switch in accordance with claim 16, wherein each of said plurality of outputs of said plurality of first switch circuits, outputs a respective one of a plurality of data signals, said data signals being time-division multiplexed.

21. A switch in accordance with claim 20, wherein each of said plurality of data signals includes a plurality of groups of time slots, each of said plurality of groups of time slots further including a plurality of subgroups of time slots.

22. A switch in accordance with claim 16,

wherein a number of said first switch circuits is 32 and said first switch circuits have a total of 384 inputs each,

wherein the number N of said second switch circuits is 22, and

wherein a number of said third switch circuits is 32 and said third switch circuits have a total of 384 outputs each.

23. A switch in accordance with claim 16, wherein each of said plurality of outputs of said plurality of first switch circuits, outputs a respective one of a plurality of data signals, said data signals being multiplexed.

24. A switch in accordance with claim 23, wherein said each of said plurality of data signals includes a plurality of groups, each of said plurality of groups further including a plurality of subgroups.

25. A rearrangeable, non-blocking, three-stage switch configured as a Clos network, said switch comprising:

a plurality of physical center stage switch circuits, a number of said plurality of physical center stage switch circuits equaling N, where N is an integer other than a power of 2;

a plurality of logical center stage switch circuits equaling N*f, where f is a number of logical center stage switch circuits per physical center stage switch circuit, wherein the plurality of physical center stage switch circuits are configured into the plurality of logical center stage switch circuits; and

a subset of the plurality of logical center stage switch circuits equaling n, where n is less than N*f and n is a power of 2.

26. The switch of claim 25 wherein the subset of the plurality of logical center stage switch circuits carries data signals.

27. The switch of claim 25 wherein at least some of said plurality of physical center stage switch circuits are configured as the plurality of logical center stage switch circuits based upon solving the following equations:

1) B<=N*T, where B is an input bandwidth to be switched by a first stage switch circuit, which is coupled to the plurality of physical center stage switch circuits; N is the number of the plurality of physical center stage switch circuits; T is the available bandwidth between the first stage switch circuit and one of the plurality of physical center stage switch circuits; and

2) B<=†N*f†* t/f; f is an integer factor of a number t, where t is the available bandwidth that will be used by the switch and t<=T, and †N*f† is a highest power of 2 less than N*f.

28. The switch of claim 25 wherein T is measured in bandwidth units.

29. The switch of claim 28 wherein the bandwidth unit is a timeslot.

30. The switch of claim 28 wherein t is a number of timeslots.

31. The switch of claim 25 wherein each of the plurality of physical center stage switch circuits is comprised of a second three-stage switch.

32. A method for configuring a three-stage switch, the method comprising the steps of:

setting a value for N, where N equals a number of a plurality of physical center stage switch circuits of the switch;

setting a value for B, where B is an amount of input bandwidth to be switched by a first stage switch circuit of the switch;

setting a value for T, where T is an available bandwidth between the first stage switch circuit and one of the plurality of physical center stage switch circuits;

solving for f in an equation, where f is an integer factor of a number t, where t is the available bandwidth that will be used by the switch and t<=T,

wherein the equation includes:

B<=N*T and

B<=⌊N*f⌋* t/f, where ⌊N*f⌋is the highest power of 2 less than N*f.

33. A computer readable medium for storing a method to be executed by a processor, wherein the method comprises the steps of:

setting a value for N, where N equals a number of a plurality of physical center stage switch circuits of the switch;

setting a value for B, where B is an amount of input bandwidth to be switched by a first stage switch circuit of the switch;

setting a value for T, where T is an available bandwidth between the first stage switch circuit and one of the plurality of physical center stage switch circuits;

solving for f in an equation, where f is an integer factor of a number t, where t is the available bandwidth that will be used by the switch and t<=T,

wherein the equation includes:

B<=N*T and

B<=⌊N*f⌋* t/f, where ⌊N*f⌋is the highest power of 2 less than N*f.

REMARKS

Claims 1-15 are pending in the present application. Claims 1-15 have been cancelled and claims 16-31 have been added. Claims 16, 25, 32 and 33 are independent.

Entry of the above amendments is earnestly solicited. An early and favorable first action on the merits is earnestly solicited.

Conclusion

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0308 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact Michael R. Cammarata (Reg. 39,491) at the 410-694-5763.

Respectfully submitted,

Dated: Dec 17, 2001

By: _____
Michael R. Cammarata
Reg. 39,491

CIENA Corporation
Legal Department
1201 Winterson Road
Linthicum, MD 21090
Phone: (410) 694-5763
Fax: (410) 865-8001
Pager: (877) 502-5736

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE TITLE OF THE INVENTION:

Please amend the title as follows:

REARRANGEABLE SWITCH [BASED ON THE LOOPING ALGORITHM AND] HAVING A NON-POWER OF TWO NUMBER OF PHYSICAL CENTER STAGES

\

IN THE ABSTRACT OF THE DISCLOSURE:

Please replace the abstract with the following:

-- A switch is provided that includes three stages. The first stages has a plurality of switch circuits. The second stage has a plurality of switch circuits equal to N, where N is any integer other than a power of 2 and where the switch circuits can be logically configured into a logical configuration of a power of 2. The third stages includes a plurality of switch circuits. --

IN THE SPECIFICATION:

Please amend the specification as follows:

On page 4, the first and second full paragraphs are amended as follows:

--Fig. 1 illustrates a switch 100 consistent with an embodiment of the present invention. Switch 100 includes a plurality of inputs 110-1 to 110-256, which receive

signals conforming to a given protocol from an external network; group the signals in frames suitable for processing in switch [200] 100; and forward the signals to a first stage of switch circuits 112-1 to 112-32. The data signals are routed through these switch circuits and passed to a second stage of switch circuits 114-1 to 114-22, which further route the data signals. A third stage of switch circuits 116-1 to 116-32 direct the data to desired outputs 118-1 to 118-256, which supply the data signals to an external network, but typically in the protocol in which the signals were input to switch 100.

Fig. 2 illustrates input 110-1 in greater detail. Remaining inputs 110-2 to 110-256 typically have a similar construction as input 110-1. Data is generally supplied to input 110-1 as optical signals conforming to a Synchronous Optical Network (SONET) protocol at a rate of approximately 2.5 Gbit/sec. A receiver circuit, including for example, photodetector 210 converts the received optical signals into corresponding electrical signals. A conventional clock and data recovery circuit 212 appropriately shapes the electrical signals and extracts a clock signal for timing purposes. A framer circuit is coupled to the output of the clock and data recovery circuit, for grouping the received data into frames suitable for processing within switch [200] 100. --

On page 5, the second and third full paragraphs are amended as follows:

--By way of introduction, switches can be classified into one of two categories, space division and time division. Space division switches can be implemented as crossbar switches having m input and n outputs and mn crosspoints (m and n [and] are integers). By making an electrical contact via a crosspoint between a horizontal input bus and a vertical output bus, a connection can be made between the associated input and

output, respectively.

Instead of using a space division switch, however, time division switching techniques can also be applied for interconnecting inputs and outputs. A so-called time slot interchanger (TSI) can be used for such purposes. A TSI includes a buffer which reads from a single input and writes to a single output. The input is framed into m fixed-length time slots. The information in each input time slot is read sequentially into consecutive time slots (cyclically) of a buffer of m slots. The output is framed into n time slots, and information from the appropriate slot in the buffer is transmitted [on to] onto a corresponding output slot. Thus, over the duration of an output frame, the content of the buffer is read in predetermined manner according to a read-out sequence so that the information in each slot of the input frame is rearranged into the appropriate slot in the output frame. As a result, each time slot is interchanged. ---

On page 6 and 7, please replace the full paragraph beginning at the bottom of page 6 and ending at the top of page 7 with the following paragraph:

-- An example of the steps carried out by the Looping Algorithm will next be described with reference to Fig. 4(c). In a first step, an unconnected input of 2 x 2 switch 420 in stage 406 is coupled, via upper switch 402, to desired output of 2 x 2 switch [422] 423 in stage 408. The adjacent output of switch [422] 423 is then coupled to a desired input, e.g., [the remaining] an input of switch [420] 421, through lower switch 404. [Another] The 2 x 2 switch 421 in stage 406 then is [then selected, connections are made] coupled to the adjacent input of switch 421 through the upper switch 402 (loop forward)[,] to an

output of switch 422 in stage 408. [; and an] An adjacent output of switch 422 is coupled to an input of [stage 406] switch 420 through lower switch 404 (loop back). This process is repeated until [all] both inputs of switch 420 are connected [coupled] to corresponding outputs [of switch 400]. This completes the loop of the Looping Algorithm. Next, another unconnected input of a 2 x 2 switch in stage 406 is chosen and the above referenced steps are repeted to complete the loop. When no more unconnected inputs are free, the Algorithm terminates. --

On page 8, the first full paragraph is amended as follows:

--Fig. 6 illustrates one of the switch banks shown in Fig. 5. Each bank includes two sub-stages [620 and 630] 610 and 620 that have P 2 x 2 switches, where P is the width of the bus coupled to the inputs of each bank, e.g. P = 384 for the bank of stage 510, 192 for the banks of stage 512, 96 for the banks of stage 514, 48 for the banks of stage 516, 24 for the banks of stage 518, and 12 for the banks of stage 520. Connections between each of the 2 x 2 switches are further illustrated in Fig. 6. These connections are consistent with the requisite hardware connections within each of switch circuits 112-1 to 112-32.--